	Application No.	Applicant(s)
Notice of Allowability	10/806,093	GUETTAF, AMAR
	Examiner	Art Unit	
	Steven D. Radosevich	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *9/11/07*.

2. ☒ The allowed claim(s) is/are *1-7,9-20 and 22-28*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some*   c) ☐ None   of the:

        1. ☐ Certified copies of the priority documents have been received.

        2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

        3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
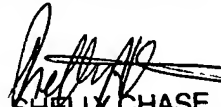
    * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

    (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

        1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____ .

    (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)

2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)

3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____

4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application

6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .

7. ☐ Examiner's Amendment/Comment

8. ☒ Examiner's Statement of Reasons for Allowance

9. ☐ Other _____ .

SHELLY CHASE
PRIMARY EXAMINER

DETAILED ACTION

Claims 1-28 are present within this instant examination. Acknowledgment is made that claims 8 and 21 have been canceled by the applicant prior to this examination and as such these claims will not be given further consideration within this instant examination.

Priority

Acknowledgment is made that no priority, either foreign or domestic is claimed for this application and as such the filing date, 3/23/2004, is being used for this examination.

Drawings

Acknowledgment is made that the figures are accepted as they appear at this time since there do not appear to be any issues that would require an objection and/or correction.

Information Disclosure Statement

Acknowledgment is made that an Information Discloser Statement (IDS) was provided prior to this instant examination, on 09/11/2007, and as such the contents of that IDS has been fully reviewed and considered.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michael D. Specht on 11/26/07.

The application has been amended as follows:

1. In scan testing of an integrated circuit with a plurality of scan paths, a method for debugging scan testing failures of the integrated circuit, comprising the steps of:

    (a) conducting scan tests on the plurality of scan paths;

    (b) identifying a bad scan path that is generating one or more errors within the plurality of scan paths, wherein all other scan paths within the plurality of scan paths are considered to be good scan paths;

    (c) assessing test results on the bad scan path and good scan paths;

    (d) masking the bad scan path to define a segment point that segments the bad scan path into two segments;

    (e) tracing the source of errors in the bad scan path segment following the segment point when the number of errors of an output of the bad scan path following the segment point are less than a bad path error threshold and the number of errors of outputs on each of the good scan paths are less than a good path error threshold; and

    (f) shifting the segment point based on an analysis of the errors generated by the bad scan path and the good scan paths and returning to step (d) when the number of errors of an output of the bad scan path are greater than a bad path error threshold or the number of errors on an

output of the bad scan path do not exceed the bad scan path error threshold and the number of errors on an output of any of the good scan paths is greater than a good scan path error threshold.

17. In scan testing of an integrated circuit with a plurality of scan paths, a method for debugging scan testing failures of the integrated circuit, comprising the steps of:

(a)   conducting scan tests on the plurality of scan paths;

(b)   identifying a plurality of bad san paths that are generating one or more errors within the plurality of scan paths, Wherein all other scan paths within the plurality of scan paths are considered to be good scan paths;

(c)   assessing scan test results on the bad scan paths under test and good scan paths;

(d)   masking all bad scan paths except a bad scan path under test, which had not been through steps (e) through (g);

(e)   masking the bad scan path to define a segment point that segments the bad scan path into two segments;

(f)   tracing the source of errors in the bad scan path segment following the segment point when the number of errors of an output of the bad scan path following the segment point are less than a bad path error threshold and the number of errors of outputs on each of the good scan paths are less than a good path error threshold;

(g)   shifting the segment point based on an analysis of the errors

generated by the bad scan path and the good scan paths and returning to

step (e) when the number of errors of an output of the path scan path

under test are greater than a bad path error threshold or the number of

errors on an output of the bad scan path do not exceed the bad scan path

error threshold and the number of errors on an output of any one of the

good scan paths are greater than a good scan path error threshold; and

(h)   repeating steps (d) through (g) until the source or sources of errors

within all the bad scan paths among said plurality of bad scan paths have

been located.

Allowable Subject Matter

The following is and examiner's statement of reasons for allowance:

Claims 1-7, 9-20, and 22-28 allowable.

The present invention pertains to debugging identified faulty scan paths through

the use of masking and considered non-faulty scan paths in-order to trace (locate) the

source of errors within the faulty scan path. The claimed invention recites features such

as: "... (a) conducting scan tests on the plurality of scan paths; (b) identifying a bad

scan path that is generating one or more errors within the plurality of scan paths,

wherein all other scan paths within the plurality of scan paths are considered to be good

scan paths; (c) assessing scan test results on the bad scan path and the good scan

paths; (d) masking the bad scan path to define a segment point that segments the bad

scan path into two segments; (e) tracing the source of errors in the bad scan path

segment following the segment point when the number of errors of an output of the bad

scan path following the segment point are less than a bad scan path error threshold and

the number of errors or output on each of the good scan paths are less than a good

path error threshold; and (f) shifting the segment point based on an analysis of the

errors generated by the bad scan path and the good scan paths and returning to step

(d) when the number of errors f an output of the bad scan path are greater than a bad

scan path error threshold of the number of errors on an output of the bad scan path do

not exceed the bad scan path error threshold and the number of errors on an output of

any one of the good scan paths is greater than a good path error threshold."

None of the prior arts of record, either taken by itself or in any combination,

would have anticipated or more obvious the following limitations combined with the

above limitations at or before the time the invention was filed: "... (a) conducting scan

tests on the plurality of scan paths; (b) identifying a bad scan path that is generating one

or more errors within the plurality of scan paths, wherein all other scan paths within the

plurality of scan paths are considered to be good scan paths; (c) assessing scan test

results on the bad scan path and the good scan paths; (d) masking the bad scan path to

define a segment point that segments the bad scan path into two segments; (e) tracing

the source of errors in the bad scan path segment following the segment point when the

number of errors of an output of the bad scan path following the segment point are less

than a bad scan path error threshold and the number of errors or output on each of the

good scan paths are less than a good path error threshold; and (f) shifting the segment

point based on an analysis of the errors generated by the bad scan path and the good

scan paths and returning to step (d) when the number of errors f an output of the bad

scan path are greater than a bad scan path error threshold of the number of errors on

an output of the bad scan path do not exceed the bad scan path error threshold and the

number of errors on an output of any one of the good scan paths is greater than a good

path error threshold."

Any comments considered necessary by applicant must be submitted no later

than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on

Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Steven D. Radosevich whose telephone number is 571-

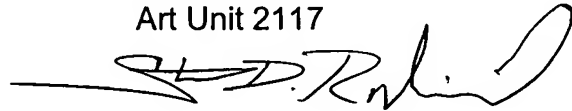272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Jacques H. Louis can be reached on 571-272-6962. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2117

SHELLY CHASE
PRIMARY EXAMINER